

**FEATURES**

- Double Side Cooling
- High Surge Capability

**APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

**VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR2150C42	4200	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 200\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR2150C40	4000	
DCR2150C35	3500	
DCR2150C30	3000	

Lower voltage grades available.

**ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

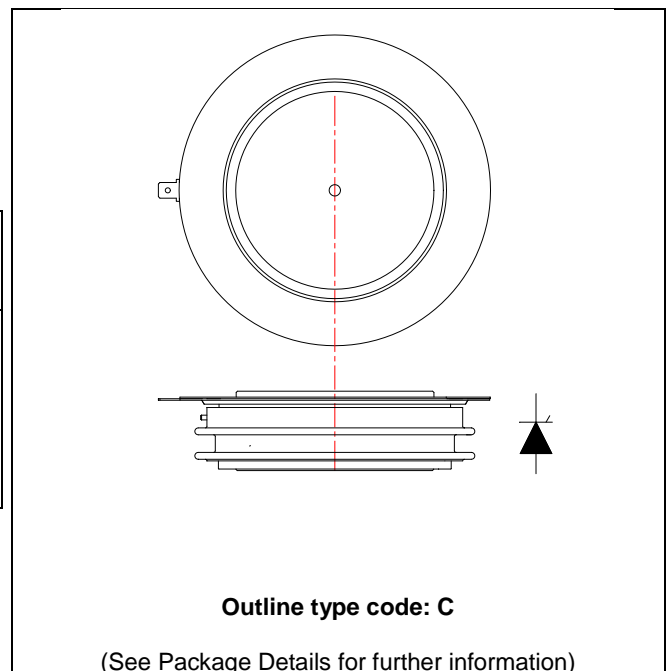
**DCR2150C42**

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

**KEY PARAMETERS**

$V_{DRM}$	<b>4200V</b>
$I_{T(AV)}$	<b>2150A</b>
$I_{TSM}$	<b>29000A</b>
$dV/dt^*$	<b>1500V/<math>\mu\text{s}</math></b>
$dI/dt$	<b>400A/<math>\mu\text{s}</math></b>

\* Higher  $dV/dt$  selections available



**Fig. 1 Package outline**

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2150	A
$I_{T(RMS)}$	RMS value	-	3377	A
$I_T$	Continuous (direct) on-state current	-	3280	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	29.0	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	4.2	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

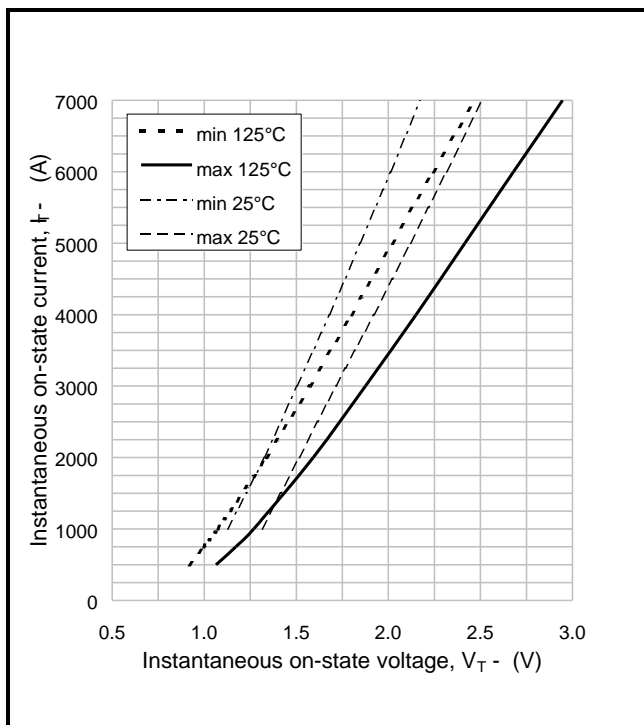
Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0101	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0176	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0239	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 37kN (with mounting compound)	Double side	-	0.0025	$^{\circ}\text{C/W}$
			Single side	-	0.005	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		33.0	41.0	kN	

**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	200	mA	
$dV/dt$	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
$di/dt$	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	200	A/ $\mu s$
		Gate source 30V, 10 $\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	400	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	500A to 2000A at $T_{case} = 125^{\circ}C$	-	0.9	V	
	Threshold voltage – High level	2000A to 7000A at $T_{case} = 125^{\circ}C$	-	1.08	V	
$r_T$	On-state slope resistance – Low level	500A to 2000A at $T_{case} = 125^{\circ}C$	-	0.36	m $\Omega$	
	On-state slope resistance – High level	2000A to 7000A at $T_{case} = 125^{\circ}C$	-	0.265	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	-	3	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $V_R = 200V$ , $di/dt = 1A/\mu s$ , $dV_{DR}/dt = 20V/\mu s$ linear	250	500	$\mu s$	
$Q_S$	Stored charge	$I_T = 2000A$ , $T_j = 125^{\circ}C$ , $di/dt = 1A/\mu s$ ,	1000	3000	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	350	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

**CURVES**

**Fig.2 Maximum & minimum on-state characteristics**
**V<sub>TM</sub> EQUATION**

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

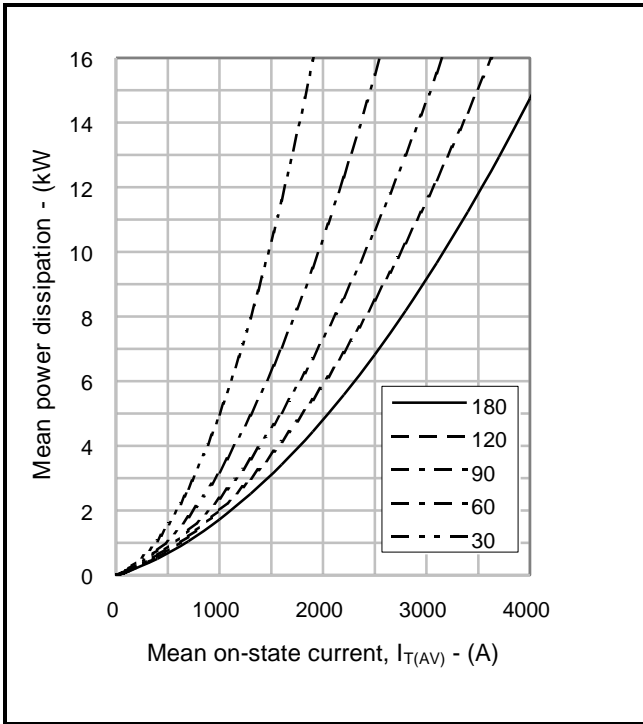
Where A = 0.137154

B = 0.132631

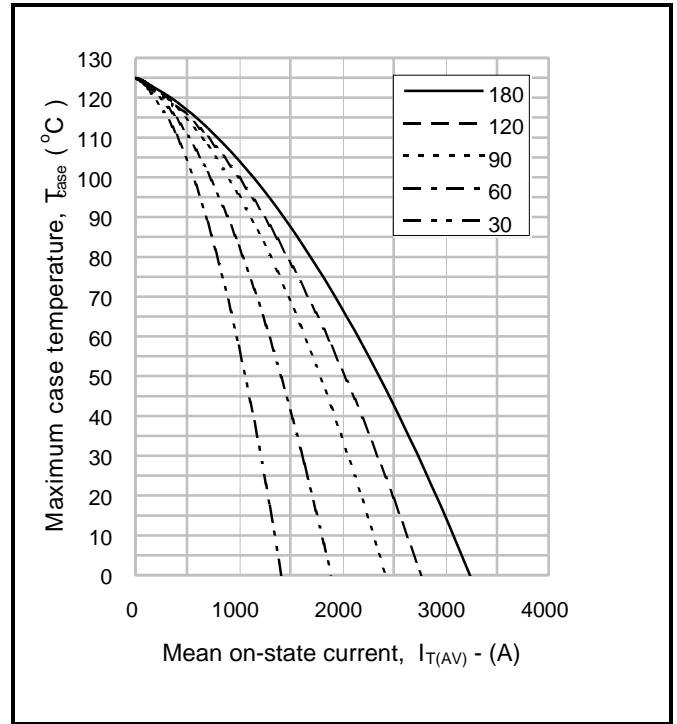
C = 0.000248

D = -0.001126

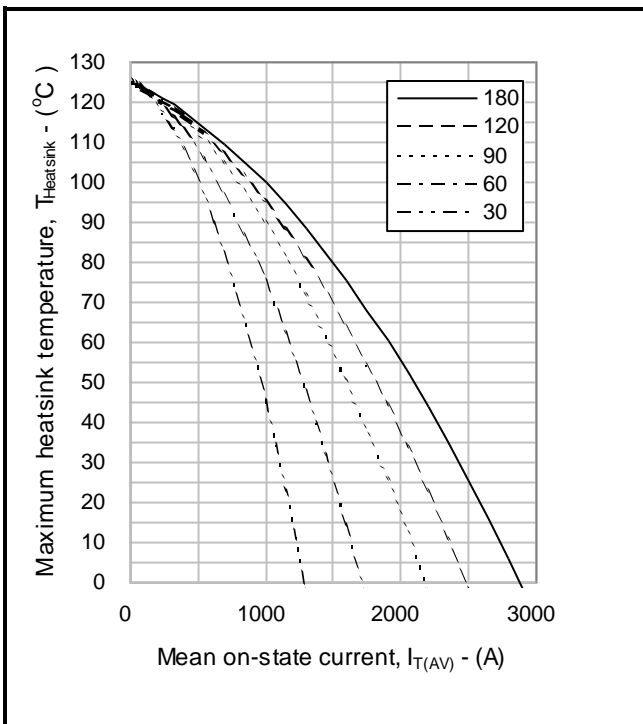
 these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 100A to 7000A



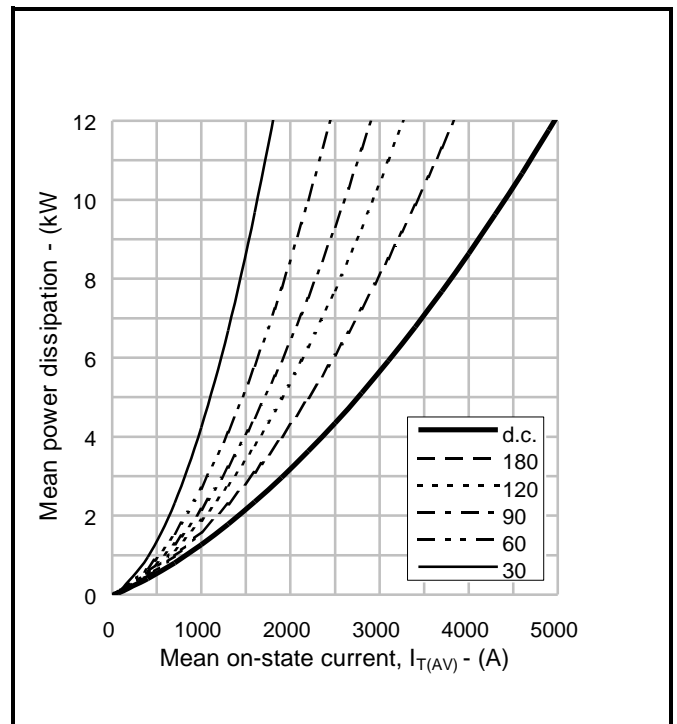
**Fig.3 On-state power dissipation – sine wave**



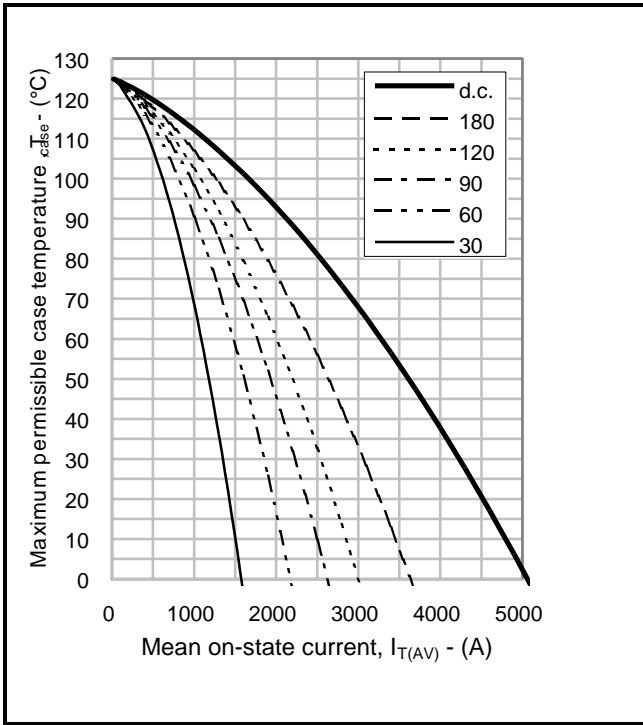
**Fig.4 Maximum permissible case temperature, double side cooled – sine wave**



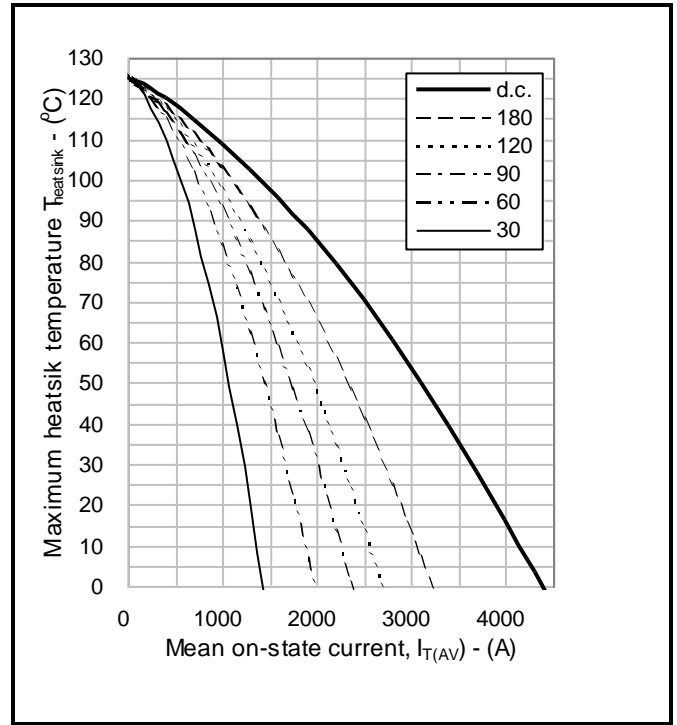
**Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave**



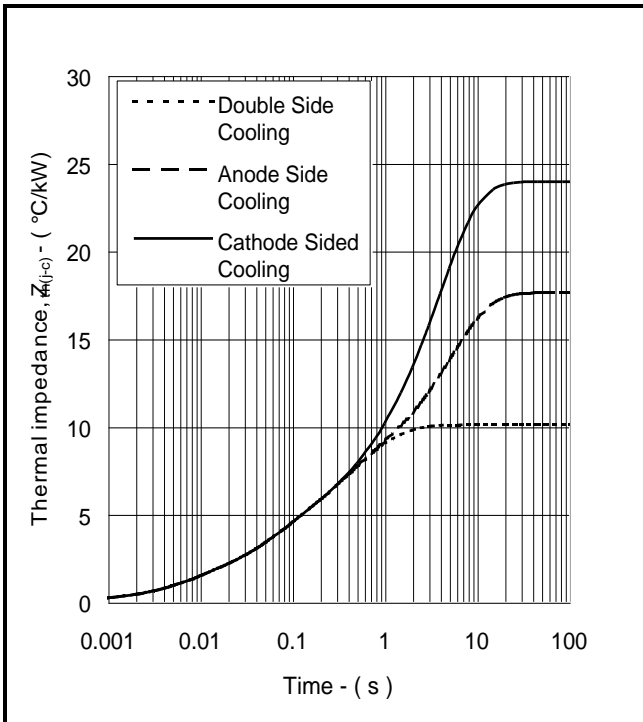
**Fig.6 On-state power dissipation – rectangular wave**



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	1.1043	2.576	4.5096	1.9009
	T <sub>i</sub> (s)	0.006176	0.0517916	0.3820376	1.06
Anode side cooled	R <sub>i</sub> (°C/kW)	1.0977	2.4566	4.0469	9.9994
	T <sub>i</sub> (s)	0.006153	0.050142	0.3129407	5.27
Cathode side cooled	R <sub>i</sub> (°C/kW)	1.1519	2.8926	2.4064	17.4793
	T <sub>i</sub> (s)	0.006389	0.0582953	0.3775516	3.97

$$Z_{th} = \sum [R_i \times (1 - \exp. (-t/t_i))] \quad [1]$$

**ΔR<sub>th(j-c)</sub> Conduction**

Tables show the increments of thermal resistance R<sub>th(j-c)</sub> when the device operates at conduction angles other than d.c.

θ°	Double side cooling		Anode Side Cooling		Cathode Sided Cooling	
	ΔZ <sub>th</sub> (z)		ΔZ <sub>th</sub> (z)		ΔZ <sub>th</sub> (z)	
	sine.	rect.	sine.	rect.	sine.	rect.
180	1.95	1.26	1.95	1.26	1.95	1.26
120	2.32	1.89	2.32	1.89	2.31	1.88
90	2.74	2.27	2.74	2.27	2.72	2.26
60	3.14	2.70	3.14	2.70	3.12	2.68
30	3.46	3.19	3.46	3.19	3.43	3.17
15	3.61	3.47	3.62	3.47	3.58	3.44

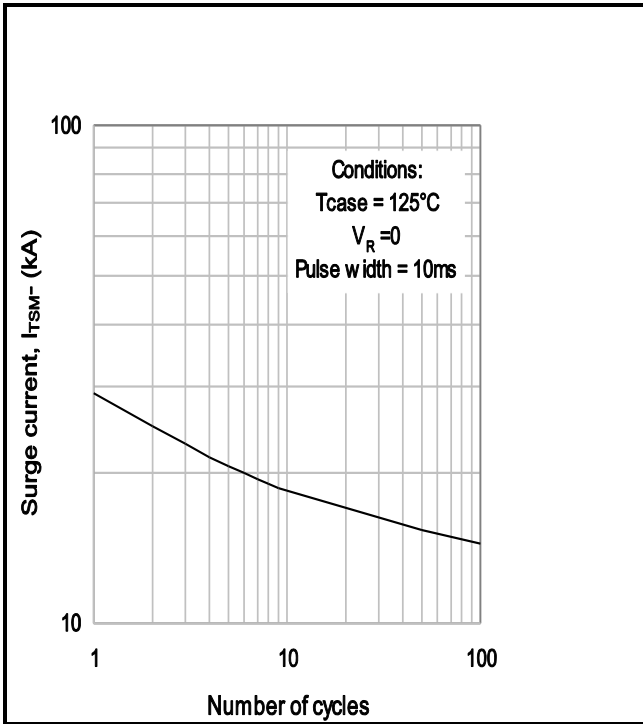


Fig.10 Multi-cycle surge current

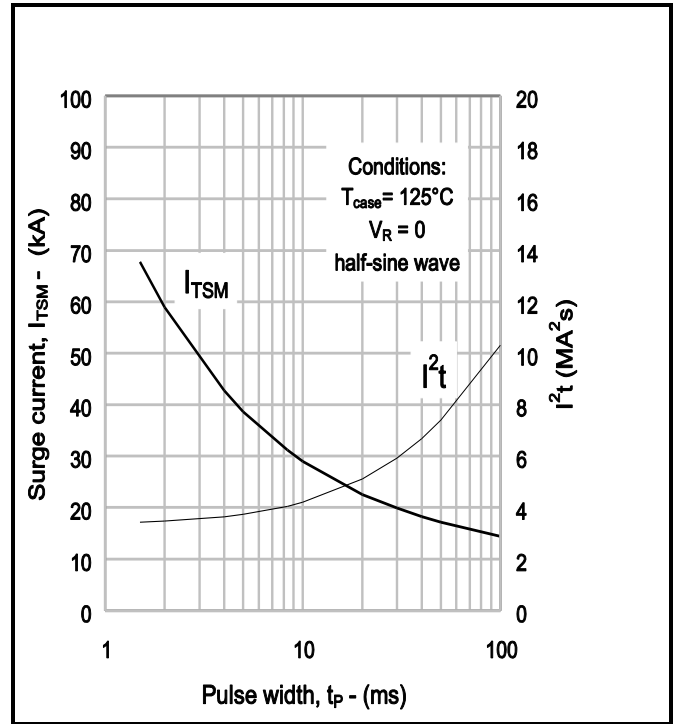


Fig.11 Single-cycle surge current

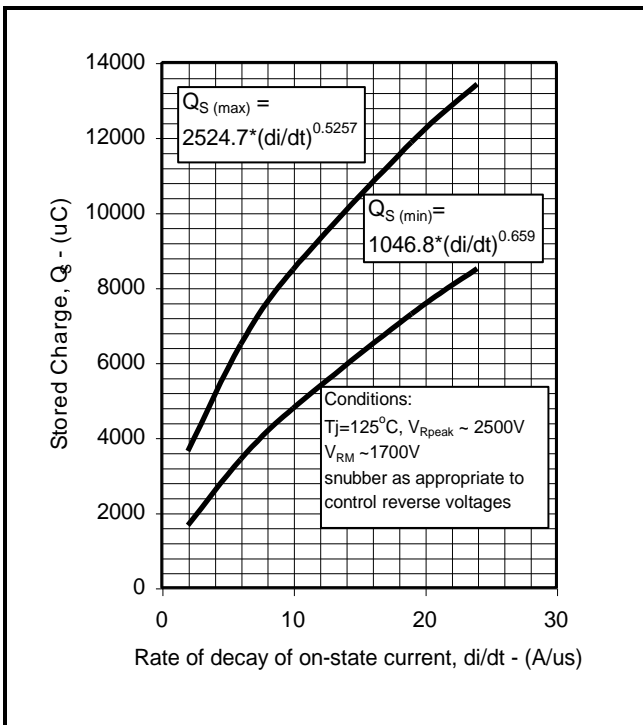


Fig.12 Reverse recovery charge

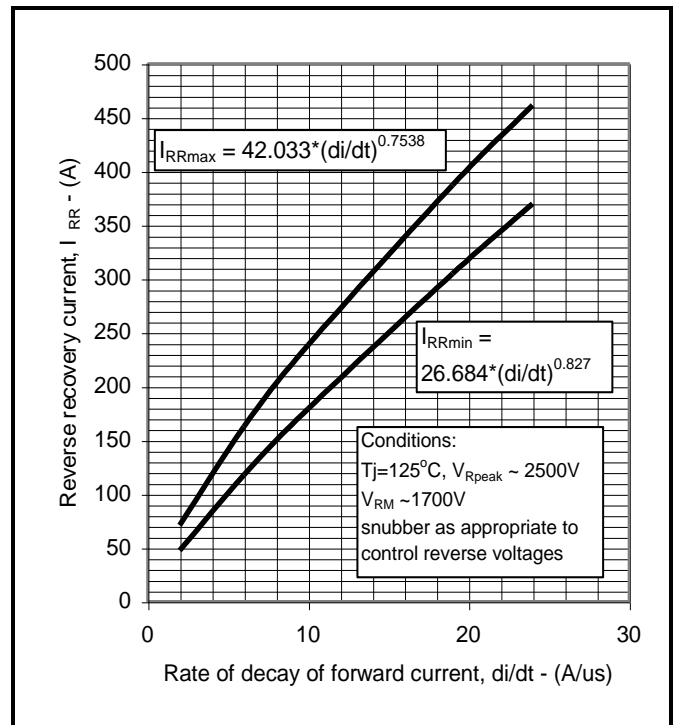
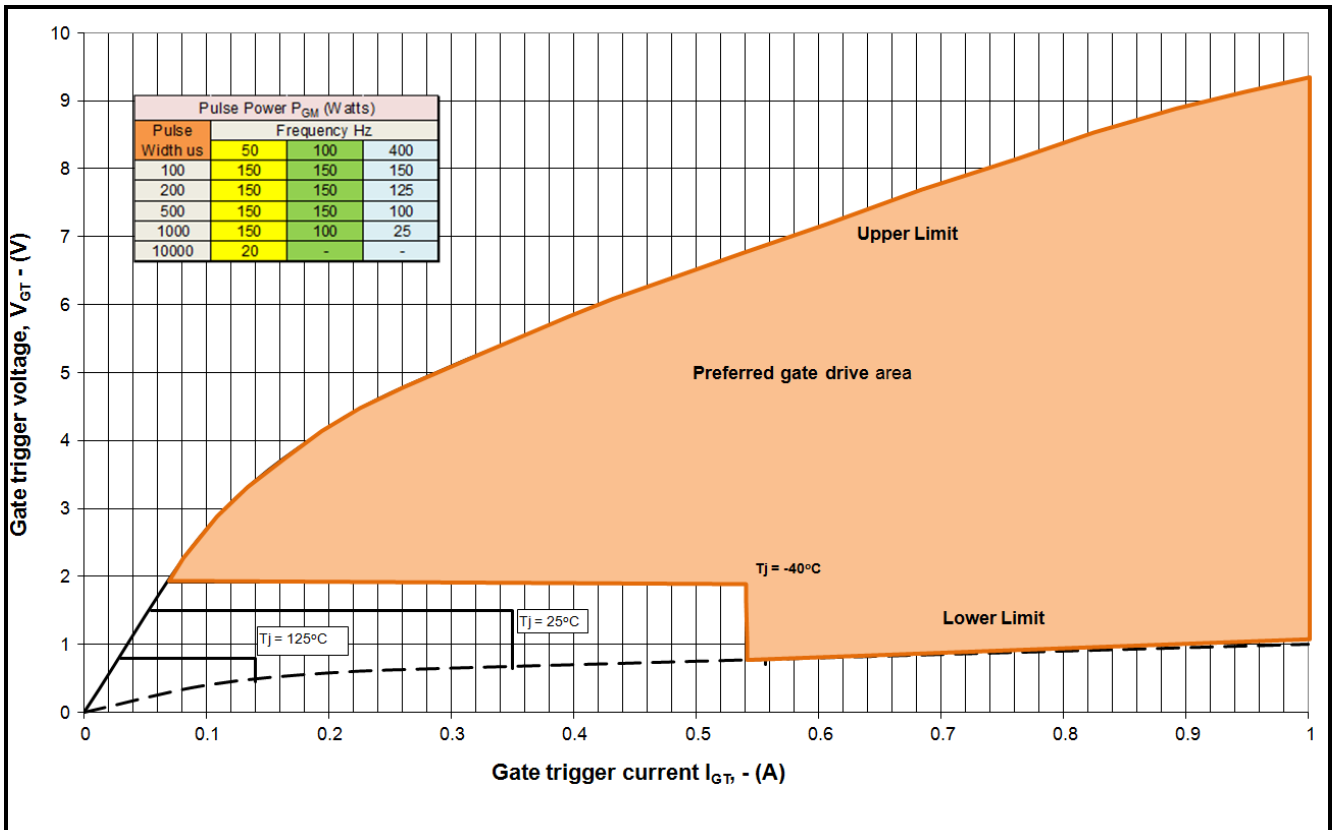
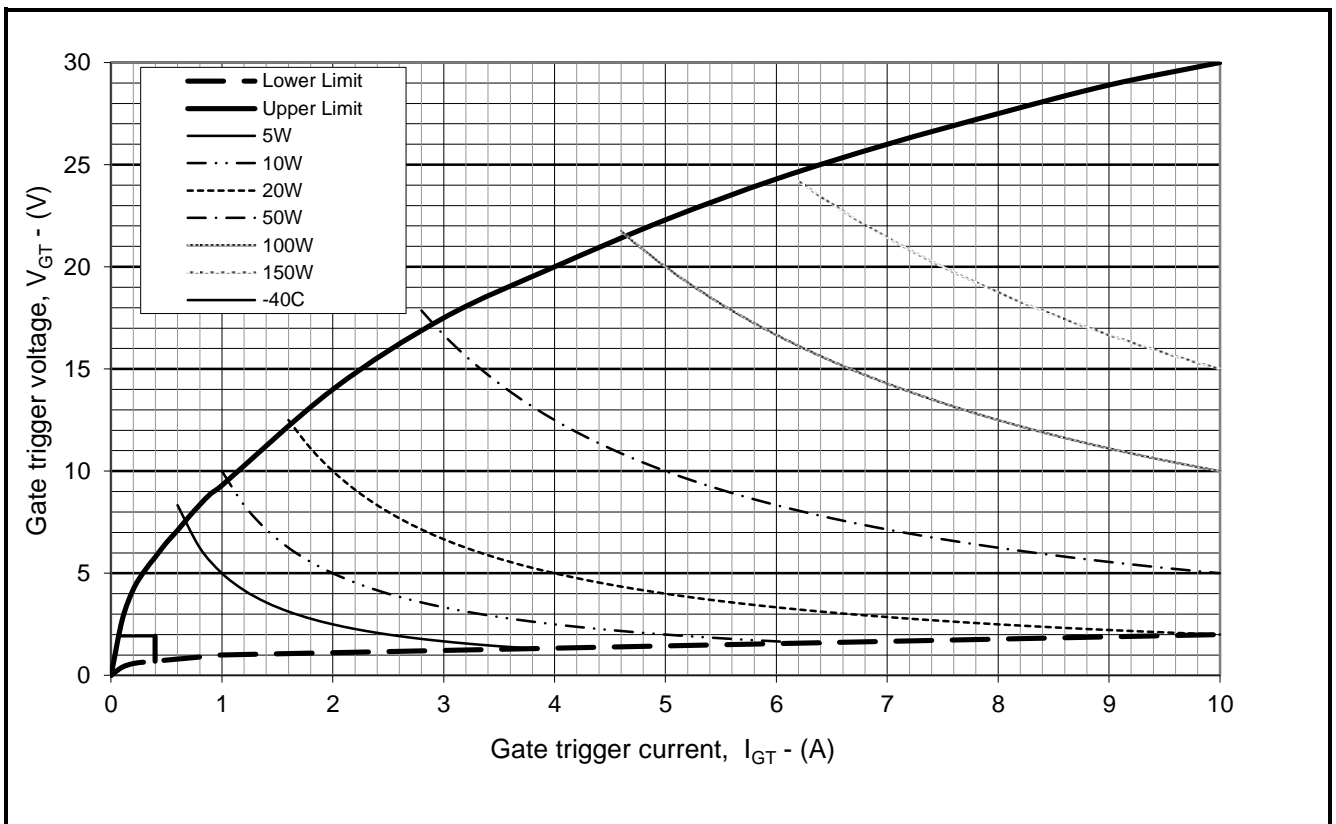


Fig.13 Reverse recovery current



**Fig14 Gate Characteristics**

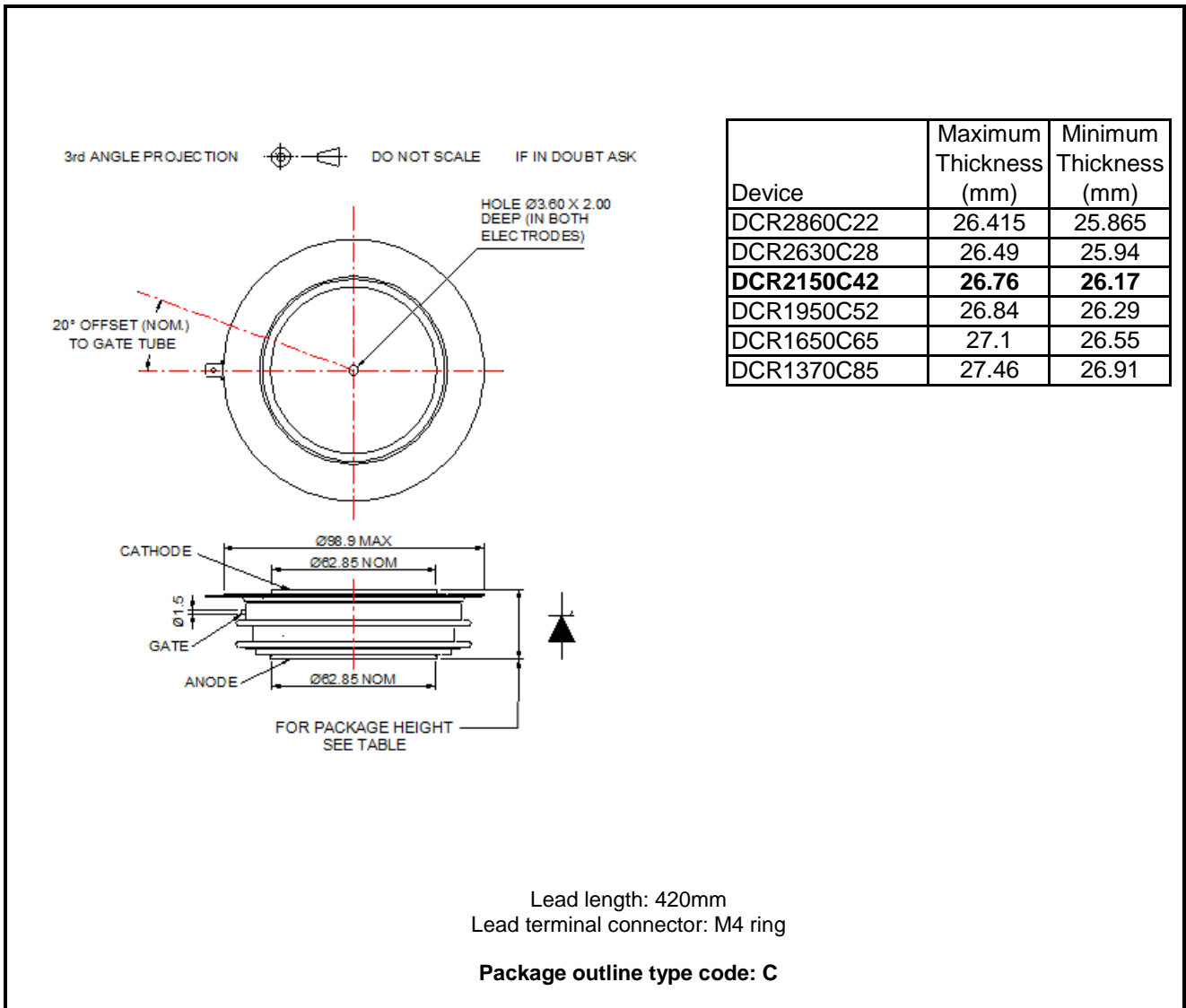


**Fig. 15 Gate characteristics**



**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. **DO NOT SCALE.**



**Fig.16 Package outline**

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